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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,122	05/08/2001	Martin Czech	Micronas.6158	4157

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,122	CZECH ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 13-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 6-8 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Jun et al. (U.S. Patent No. 6,344,385 B1).

Jun et al. disclose an ESD protective structure that protects an integrated semiconductor circuit connected between a first potential bus with a first supply potential and a second potential bus with a second supply potential, the electrostatic discharge protective structure comprising:

a laterally formed electrostatic discharge diode having a first region 13 doped with a first conduction type N and a second region 36 spaced apart from the first region 13, the second region doped a second conduction type P (figure 3a);

wherein the electrostatic discharge protective structure is located between the first 34 and second potential busses (ground) and drains off an overvoltage pulse to one of the first and second potential busses (figure 3a); and

wherein the laterally formed electrostatic discharge diode includes a gate electrode 35 located between the first region 13 and the second region 36, the first

region being separate from the second region by a distance that is equal to a width of the gate (figure 3a).

With regard to claim 2, the protective structure includes a semiconductor body 11 having a surface in which the first and second regions are embedded (figure 3a), wherein the first region is connected via a first electrode to the first potential bus and the second region is connected via a second electrode to the second potential bus (figure 3a).

With regard to claim 3, the semiconductor body 11 includes charge carriers of the second conduction type P and the gate electrode and second electrode are connected to the second potential bus (figure 3a).

With regard to claim 6, the integrated semiconductor circuit is configured and arranged as an MOS or CMOS circuit (figure 3a, the circuit protects the MOS transistor form from source and drain 31 and 32 and gate 33).

With regard to claim 7, Jun et al. further disclose a gate dielectric that spaces the semiconductor body at a distance from the gate electrode (figure 3a).

With regard to claim 8, the gate dielectric contains silicon dioxide and the gate electrode contains polysilicon. The gate 35 is formed the same as the gate 33 of the MOS transistor, and thus discloses the same polysilicon gate and silicon dioxide gate dielectric (col. 3 line 12-35).

With regard to claim 13, Jun et al. disclose an integrated circuit with electrostatic discharge protection comprising:

a circuit (MOS transistor formed by 31,32,33) to be protected (figure 3a);

an electronic discharge device 28 that is disposed electrically parallel to the circuit to be protected between first 34 and second (ground) voltage busses, wherein the electrostatic discharge device includes a laterally shaped electrostatic discharge diode including:

a first region 13 doped with a first conduction type material P within a substrate 11 (figure 3a);

a second region 36 doped with a second conduction type material P within the substrate (figure 3a); and

a gate electrode 35 having a width W and located between the first 13 and second 36 regions such that the first and second regions are separated by the width W (figure 3a).

With regard to claim 14, Jun et al. further disclose a gate oxide disposed on the substrate between the first and second conduction regions and underlying the gate electrode (figure 3a, the gate is disclosed as MOS gate, thus containing an oxide between the gate and the substrate).

With regard to claim 15, Jun et al. do not explicitly disclose an first electrode on the substrate overlying the first region or a second electrode overlying the substrate in the second region. However, Jun et al. do disclose the first region being connected to the first voltage bus and the second region being connected to the second bus. In showing the electrical connection from the substrate to the busses, Jun et al. is implicitly disclosing electrodes to form the connections. One would recognize that electrodes would inherently be formed to provide the electrical connection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jun et al. (U.S. Patent No. 6,344,385 B1).

Jun et al. disclose all the limitations of claim 2 from which claim 4 depends. Jun et al. further teach the semiconductor body includes charges of the first conductivity type. Jun et al. do not further teach at least one well of the second conductivity type embedded in the semiconductor body and the first and second regions are embedded in the well. Nonetheless, this limitation is considered obvious. It would have been obvious to one of ordinary skill in the art at the time of the invention to form the diode of Jun et al. (including the first and second regions) in a well in the substrate to provide improved isolation from other devices on the substrate.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jun et al. (U.S. Patent No. 6,344,385 B1) as applied to claims 1-3, 6-8 and 13-15 above, and further in view of Williams (U.S. Patent No. 6,060,752).

Jun et al. do not teach the second region laterally enclosing the first region.

Williams teach an electrostatic discharge device including diodes. Williams teach in figure 11A-G various configurations of the first (P) and second (N) regions where the second region laterally encloses the first region.

Jun et al. and Williams are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the second region to laterally enclose the first region. The motivation for doing so is to provide improved carrier confinement. Therefore, it would have been obvious to combine Jun et al. with Williams to obtain the invention of claim 5.

6. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun et al. (U.S. Patent No. 6,344,385 B1) in view of Voldman et al. (U.S. Patent No. 6015993).

With regard to claim 16, Jun et al. disclose an integrated circuit with electrostatic discharge protection comprising:

a circuit (MOS transistor formed by 31,32,33) to be protected (figure 3a);

an electronic discharge device 28 that is disposed electrically parallel to the circuit to be protected between first 34 and second (ground) voltage busses, wherein the electrostatic discharge device includes a laterally shaped electrostatic discharge diode including:

a first region 13 doped with a first conduction type material P within a substrate 11 (figure 3a);

a second region 36 doped with a second conduction type material P within the substrate (figure 3a);

an insulator (not shown, but the gate is disclosed as a MOS gate, thus containing an oxide between the gate and the substrate) between the gate 35 and the substrate 11 and thus between the first and second electrodes; and

a gate electrode 35 in communication with and contiguous with the insulator and having a width equal to the width separating the first doped region and the second doped region (figure 3a).

Jun et al. do not explicitly disclose a first electrode in communication with the first region or a second electrode in communication with the second region. However, Jun et al. do disclose the first region being connected to the first voltage bus and the second region being connected to the second bus. In showing the electrical connection from the substrate to the busses, Jun et al. is implicitly disclosing electrodes to form the connections. One would recognize that electrodes would inherently be formed to provide the electrical connection.

Jun et al. do not teach the insulator (gate oxide) having an insulator dimension that is equal to the distance between the first and second regions. It is noted that the gate 35 is the same length as the distance between the first and second regions.

Voldman et al. teaches a similar integrated circuit with electrostatic discharge protection. Voldman et al. teach in figure 1A, 1B, 2, 4, 5, 6 and 7, an insulator formed between the gate and the substrate (for example, insulator 108 in figure 1A) that is formed to the same length as the gate. It is well known in the art to form the gate

insulator to the same pattern as the gate as shown in Voldman et al. This structure is common in the art because it results from the use of a single patterning step to pattern the entire gate structure (gate and insulator) so as to save on production steps, time, and cost by eliminating the need for a separate etch for the gate and the insulator. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the insulator of Jun et al. to the same dimension as the gate as shown in Voldman et al. in order to simplify processing to obtain the invention of claim 16.

With regard to claim 17, the insulator includes an oxide.

With regard to claim 18, the oxide is not specifically disclosed as silicon dioxide. However, Voldman et al. teach growing the oxide on the surface of a silicon substrate. One of ordinary skill in the art at the time of the invention would recognize that a grown silicon oxide layer would be silicon dioxide.

Response to Arguments

7. Applicant's arguments filed 8/4/04 have been fully considered but they are not persuasive.

Applicant argues that Jun et al. do not teach the width of the dummy polysilicon layer 35 is equal to the distance between the first and second region. This is not persuasive as Jun et al. clearly show this feature in figure 3a. The fact that Jun et al. also teach that the channel length can be adjusted does not change the fact that figure 3a shows the two lengths as equal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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